

1890-0215

**REMARKS****I. Status of the Application**

Claims 14-34 are pending in this application. In the September 27, 2007 office action, the Examiner:

- A. Rejected claims 22-25 and 33 as being anticipated under 35 U.S.C. § 102(b) by U.S. Patent No. 6,519,165 to Koike;
- B. Rejected claims 14-16 and 26-29 as being obvious and unpatentable under 35 U.S.C. § 103 over U.S. Patent No. 6,563,720 to Kitano (hereinafter "Kitano");
- C. Rejected claims 17 and 30 as being obvious and unpatentable under 35 U.S.C. § 103 over U.S. Patent No. 5,297,014 to Saito (hereinafter "Saito");
- D. Rejected claims 18, 19, 31 and 32 as being obvious and unpatentable under 35 U.S.C. § 103 over Kitano and further in view of Koike;
- E. Rejected claim 20 as being obvious and unpatentable under 35 U.S.C. § 103 over Kitano and Koike and further in view of U.S. Patent No. 6,271,707 to DiTommaso; and
- F. Allowed claim 34.

Applicants gratefully acknowledge the telephonic interview of January 8, 2008, as well as a follow-up conversation.

Please charge the \$120.00 fee required by 37 C.F.R. § 1.17(a)(1) for the Extension of Time to Deposit Account No. 13-0014. Also, please provide any further extensions of time which may be necessary and charge any fees which may be due to Deposit Account No. 13-0014, but not to include any payment of issue fees.

1890-0215

## II. Patentability of Claim 22 and 33

Claims 22 and 33 stand rejected as allegedly being anticipated by Koike. Claim 22 now recites

a current limitation circuit arranged to receive a first signal indicative of the current through the primary of the transformer and to limit the current pulses responsive to a signal that is indicative of a condition in which both the first signal indicates that the current is above a burst mode threshold value and the memory device indicates that the switching mode power supply is operating in the burst mode.

Koike clearly limits does not generate a signal that is indicative of a condition where *both* an overcurrent is detected and the memory shows the device to be in burst mode. As shown in Fig. 2 of Koike, the overcurrent detection signal on line 41a (see Fig. 1) is provided to an *or*-gate, and nowhere else. To the extent that anything indicates that a memory device indicates a “burst mode”, it is the signal from line 10a of Fig. 1 of Koike, which is derived from the an output of the mode selector. (See September 27, 2007 office action at pp.2-3). This signal on the line 10a is also provided to the *or*-gate 35 of Fig. 2 of Koike. No signal is generated that would indicate that both signals are both “on”. Thus, no signal in Koike indicates that the current is above a burst mode threshold value *and* that the switching mode power supply is operating in the burst mode. By contrast, the claimed invention recites such a signal.

An exemplary embodiment of the claimed invention is shown in Fig. 6, wherein the *and*-gate G2 provides an output signal that indicates when both an overcurrent is detected by C4, and the power supply is in burst mode as indicated by the Q output of FF1.

Accordingly, Koike fails to disclose “a current limitation circuit arranged to receive a first signal indicative of the current through the primary of the transformer and to limit the current pulses *responsive to a signal that is indicative of a condition in which both the first signal indicates that the current is above a burst mode threshold value and the memory device indicates that the switching mode power supply is operating in the burst mode.*

1890-0215

Claim 33 is allowable for substantially the same reasons.

It is noted that these amendments are in addition to those discussed at the Interview of January 8, 2008. These amendments were discussed in a follow-up telephone conference on January 16, 2008. In that follow-up conference, the Examiner discussed the need to define the claims such that they define over a device that limits current when *either* an overcurrent exists *or* a burst mode is present. The new amendments now recite that a signal actually indicates that *both* conditions are present. Thus, claims 22 and 33 would appear to be in a condition for allowance.

III. Claims 14 and 26

Claims 14 and 26 have been amended to incorporate the limitation of claim 30. The Examiner has indicated that claims 14 and 26 as amended should be allowable.

IV. Conclusion

It is respectfully submitted that the case is now in a condition for allowance. Prompt and favorable consideration is earnestly solicited.

Respectfully submitted,



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